

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)

BUR920010167US1

Application Number

09/683,733

Applicant(s)

Aday et al.

Filing Date

02/07/02

Group Art Unit

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
JAN		US20010023418A1	09/2001	Suzuki et al.	705	400	
JAN		US 6,249,776 B1	06/2001	Bajuk et al.	705	400	
JAN		5,960,417	09/1999	Pan et al.	705	400	

RECEIVED
MAR 08 2002
Technology Center 2100

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

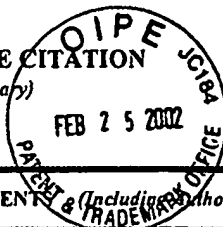
JAN	P. K. Nag, W. Maly, and H. J. Jacobs, "Simulation of Yield/Cost Learning Curves with Y4," IEEE Transactions on Semiconductor Manufacturing, vol. 10, no. 2, pp. 256 - 266, May 1997.
JAN	R. Ross, J. Bailey, N. Atchison, and M. Effron, "A Comprehensive Sequential Yield Analysis Methodology and the Financial Payback for Higher Yields," 1999 IEEE/SEMI Advanced Semiconductor Manufacturing Conference, pp. 80-86, 1999.

EXAMINER Freda J. Nelson	DATE CONSIDERED June 8, 2006
-----------------------------	---------------------------------

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)



Docket Number (Optional)

BUR920010167US1

Application Number

09/683,733

Applicant(s)

Aday et al.

Filing Date

02/07/02

Group Art Unit

*EXAMINER
INITIAL

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

SAU

C. A. Moritz, D. Yeung, and A. Agarwal, "SimpleFit: A Framework for Analyzing Design Trade-Offs in Raw Architectures," IEEE Transactions on Parallel and Distributed Systems, vol. 12, no. 7, pp. 730-742, July 2001

SAU

G. A. Allan and A. J. Walton, "Fast Yield Prediction for Accurate Costing of ICs," 1996 Innovative Systems in Silicon Conference, Session 8: Yield & Testing, pp. 279-287, 1996.

SAU

nTool Solutions, <http://www.ntool.com/ntool/Solutions/Cps/Ndiesizer/Ndiesizer.html>, printed October 8, 2001.

SAU

"UMC UNVEILS CHIPSIZER: Online Tool Estimates Die Size and Silicon Cost," <http://www.umc.com/english/news/20001030.asp>, October 30, 2000.

SAU

"UMC Chipsizer" <http://eproject.umc.com/dse/>, printed October 8, 2001.

SAU

D. N. Maynard, R. J. Rosner, M. L. Kerbaugh, R. A. Hamilton, J. R. Bentlage, and C. A. Boye, "Wafer Line Productivity Optimization in a Multi-Technology Multi-Part-Number Fabricator," 1998 IEEE/SEMI Advanced Semiconductor Manufacturing Conference, pp. 34-42, 1998.

RECEIVED
MAR 08 2002
Technology Center 2100

EXAMINER

Freda J. Olson

DATE CONSIDERED

June 8, 2006

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.